

AVC Liquid Crystal Displays Group

# LQ022B8UD05 TFT-LCD Module

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			GROUP	
		SPECIFICATION		
			_	
		DEVICE SPECIFICATION for TFT LCD Module (176 × RGB × 220 dots)		
		${ m Model}$ No. ${ m LQ022B8UD05}$		

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° Contact and consult with a SHARP sales representative for any questions about this device.

#### [For handling and system design]

(1) Do not scratch the surface of the polarizer film as it is easily damaged.

(2) If the cleaning of the surface of the LCD panel is necessary, wipe it swiftly with cotton or other soft cloth. Do not use organic solvent as it damages polarizer.

(3) Water droplets on polarizer must be wiped off immediately as they may cause color changes, or other defects if remained for a long time.

(4) Since this LCD panel is made of glass, dropping the module or banging it against hard objects may cause cracks or fragmentation.

(5) Certain materials such as epoxy resin (amine's hardener) or silicone adhesive agent (de-alcohol or de-oxym) emits gas to which polarizer reacts (color change). Check carefully that gas from materials used in system housing or packaging do not hart polarizer.

(6) Liquid crystal material will freeze below specified storage temperature range and it will not get back to normal quality even after temperature comes back within specified temperature range. Liquid crystal material will become isotropic above specified temperature range and may not get back to normal quality. Keep the LCD module always within specified temperature range.

(7) Do not expose LCD module to the direct sunlight or to strong ultraviolet light for long time.

(8) If the LCD driver IC (COG) is exposed to light, normal operation may be impeded. It is necessary to design so that the light is shut off when the LCD module is mounted.

(9) Do not disassemble the LCD module as it may cause permanent damage.

(10) As this LCD module contains components sensitive to electrostatic discharge, be sure to follow the instructions in below. ① Operators

Operators must wear anti-static wears to prevent electrostatic charge up to and discharge from human body.

2 Equipment and containers

Process equipment such as conveyer, soldering iron, working bench and containers may possibly generate electrostatic

charge up and discharge. Equipment must be grounded through 100Mohms resistance. Use ion blower. ③ Floor

Floor is an important part to leak static electricity which is generated from human body or equipment. There is a possibility that the static electricity is charged to them without leakage in case of insulating floor, so the countermeasure (electrostatic earth: $1 \times 10^8 \Omega$ ) should be made.

#### ④ Humidity

Proper humidity of working room may reduce the risk of electrostatic charge up and discharge. Humidity should be kept over 50% all the time.

(5) Transportation/storage

Storage materials must be anti-static to prevent causing electrostatic discharge.

6 Others

Protective film is attached on the surface of LCD panel to prevent scratches or other damages. When removing this protective film, remove it slowly under proper anti-ESD control such as ion blower.

(11) Hold LCD very carefully when placing LCD module into the system housing. Do not apply excessive stress or pressure to LCD module. Do not to use chloroprene rubber as it may affect on the reliability of the electrical interconnection.

(12) Do not hold or touch LCD panel to flex interconnection area as it may be damaged.

(13) As the binding material between LCD panel and flex connector mentioned in 12) contains an organic material, any type of organic solvents are not allowed to be used. Direct contact by fingers is also prohibited.

(14) When carrying the LCD module, place it on the tray to protect from mechanical damage. It is recommended to use the conductive trays to protect the CMOS components from electrostatic discharge. When holding the module, hold the Plastic Frame of LCD module so that the panel, COG and other electric parts are not damaged.



(15) Do not touch the COG's patterning area. Otherwise the circuit may be damaged.

(16) Do not touch LSI chips as it may cause a trouble in the inner lead connection.

(17) Place a protective cover on the LCD module to protect the glass panel from mechanical damages.

(18) LCD panel is susceptible to mechanical stress and even the slightest stress will cause a color change in background. So make sure the LCD panel is placed on flat plane without any continuous twisting, bending or pushing stress.

(19) Protective film is placed onto the surface of LCD panel when it is shipped from factory. Make sure to peel it off before assembling the LCD module into the system. Be very careful not to damage LCD module by electrostatic discharge when

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peeling off this protective film. Ion blower and ground strap are recommended.

(20) Make sure the mechanical design of the system in which the LCD module will be assembled matches specified viewing angle of this LCD module.

(21) This LCD module does not contain nor use any ODS (1,1,1-Trichloroethane, CCL4) in all materials used, in all production processes.

#### [For operating LCD module]

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) Do not display still picture or the display over 2 hours as this will damage the liquid crystal.

(3) As opto-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable.

#### [Precautions for Storage]

(1) Do not expose the LCD module to direct sunlight or strong ultraviolet light for long periods. Store in a dark place.

(2) The liquid crystal material will solidify if stored below the rated storage temperature and will become an isotropic liquid if stored above the rated storage temperature, and may not retain its original properties. Only store the module at normal temperature and humidity ( $25\pm5^{\circ}C$ ,  $60\pm10\%$ RH) in order to avoid exposing the front polarizer to chronic humidity.

#### (3) Keeping Method

a. Don't keeping under the direct sunlight.

b. Keeping in the tray under the dark place.



(4) Do not operate or store the LCD module under outside of specified environmental conditions.

(5) Be sure to prevent light striking the chip surface

#### [Other Notice]

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) As electrical impedance of power supply lines (VEE-VSS, VDD-VSS) are low when LCD module is working, place the de-coupling capacitor near by LCD module as close as possible.

(3) Reset signal must be sent after power on to initialize LSI. LSI does not function properly until initialize it by reset signal.

(4) Generally, at power on, in order not to apply DC charge directly to LCD panel, supply logic voltage first and initialize LSI logic function including polarity alternation. Then supply voltage for LCD bias. At power off, in order not to apply DC charge directly to LCD panel, execute Power OFF sequence and Discharge command.

(5) Don't touch to PWB surface, exposed IC chip, electric parts and other parts, to any electric, metallic materials.

(6) No bromide specific fire-retardant material is used in this module.

(7) Because including CMOS in this model, there is possibility that this module works wrongly by the noise from the antenna and so on. Please implement enough shields on user's product.

#### [Precautions for Discarding Liquid Crystal Modules]

COG : After removing the LSI from the liquid crystal panel, dispose of it in a similar way to circuit boards from electronic devices.

LCD panel : Dispose of as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal panel only contains an extremely small amount of liquid crystal (approx.100mg) and therefore it will not leak even if the panel should break.

PWB/FPC : Dispose of as similar way to circuit board from electric device.

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#### 1. Application

This data sheet is to introduce the specification of LQ022B8UD05, active matrix 262,144 colors LCD module. The LCD module controlled by Driver ICs (LR38825 / LH169CH).

If any problem occurs concerning the items not stated in this specification, it must be solved sincerely by both parties after deliberation.

As to basic specification of driver IC refer to the IC specification and handbook.

#### 2. Construction and Outline

Construction: LCD panel, Driver (COG), FPC with electric components,

4 pieces White LED lump, prism sheet, diffuser, light guide and reflector, plastic frame to fix them mechanically. Outline: See Fig.12 (page 22).

Connection: 35 pins; 0.3mm pitch ZIF FPC connector. Correspondable connector: FF02B35SS1 (JAE)

#### 3. Mechanical Specification

		Table 1	
Parameter		Specifications	Unit
Outlin	e dimensions *1	42.1 (W) × 56.6 (H) × 4.2 (D)	mm
LCD	Active area	34.848 (W) × 43.56 (H)	mm
Panel Display format		176×RGB(W)×220(H)	-
	Dot pitch	0.066 (W) ×0.198 (H)	mm
	Base color *2	Normally white	-
	Mass	Approx 12.1	g

\*1 See Fig.12 (page 22)

\*2 Due to the characteristics of the LC material, the colors vary with environmental temperature.

#### 4. Absolute Maximum Ratings

(4-1) Electrical absolute maximum ratings

	Table 2			Ta=25°C		
Parameter	Symbol	Min	Max	Unit	Remark	
Supply voltage for LCD	VEE-VSS	-0.3	4.0	V	VEE	
Supply voltage for Logic	VDD-VSS	-0.3	4.0	V	VDD	
Input Voltage	$V_{IN}$	-0.3	VDD+0.3	V	*1	
LED forward current	I <sub>LED</sub>	0	30	mA	*2	

\*1 Input terminal of logic system. : Voltage value is based on VSS = 0V.

\*2 See (5-2) LED back light (page 9)

#### (4-2) Environment Conditions

Table 3								
Item	Тор		Tstg		Remark			
	MIN. MAX. MIN. MAX.							
Ambient temperature	-10 °C	+60°C	-20 °C	+70°C	Note 2)			
Humidity	Note 1)		Note 1)		No condensation			

Note1) Ta  $\leq$  40 °C......95 % RH Max

Note2) Ta > 40 °C.....Absolute humidity shall be less than Ta=40 °C /95 % RH.

As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable. Be sure not to exceed the rated voltage, otherwise a malfunction may occur.



#### 5. Electrical Specifications

(5-1) Electrical characteristics

		Table 4		Ta=25°C, V	EE=3.0V, V	VDD=3	.0V, VSS=0V
Parameter	Symbo l	Conditions	Min.	Тур.	Max.	Unit	Applicable Pin
Supply voltage for LCD	VEE- VSS	Ta=-10 <b>~</b> 60 °C	2.8	3.0	3.2	V	VEE
Supply voltage for Logic	VDD- VSS	Ta=-10 <b>∼</b> 60 °C	1.7	3.0	3.6	v	VDD
"H" level input voltage	V <sub>IH</sub>	Ta=-10 <b>~</b> 60 °C	0.7VDD	-	-	V	(mata1)
"L" level input voltage	V <sub>IL</sub>	1a10 -00 C	-	-	0.3VDD	V	(note1)
"H" level Input leakage current	$\mathbf{I}_{\mathrm{IH}}$	Ta=-10 <b>∼</b> 60 °C	-	-	10	μΑ	
"L" level Input leakage current	I <sub>IL</sub>	V <sub>IN</sub> = VSS or VDD	-10	-	-	μΑ	(note2)
"H" level output voltage	V <sub>OH</sub>	Ta=-10 <b>~</b> 60 °C	0.8VDD	-	-	V	(
"H" level output voltage	V <sub>OL</sub>	$I_{OH}$ =-100µA, $I_{OL}$ =100µA	-	-	0.2VDD	V	(note3)
Current consumption for LCD	I <sub>EE</sub>		-	5.5	8.0	mA	
Current consumption for Logic	I <sub>DD</sub>	Ta=25 °C		2.0	10.0	μΑ	(note4)

(note1) /WR, /CS, RS, /RD, /RES, D0~D15

(note2) /WR, /CS, RS, /RD, /RES, D0~D15

- (note3) LCDINT
- (note4) Following Conditions Ta=25 °C, VDD=3.0V, VEE=3.0V, Frame frequency = 80Hz Display Pattern: All Black. No Host CPU access.





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#### (5-2) LED back light

(1) At LCD panel, the back light use 4pieces white LED.

			Tab	<u>le 5</u>			
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit	Remark
Forward current	I <sub>LED</sub>	Ta=25 °C	-	20	30	mA	CA

LED maker : NICHIA Corporation

LED type : NSSW008CT

\*Please consider Allowable Forward Current on used temperature

(refer to Ambient Temperature vs. Allowable Forward Current curve)



#### <SPECIFICATIONS>

(1) Ab	solute Maximum Ratings	Table 6		(Ta=25°C)
	Item	symbol	MAX	unit
	Forward Current	IF	35	mA
	Pulse Forward Current	IFP	100	mA
	Reverse Voltage	θy-	5	V
	Power Dissipation	$\theta y +$	123	mW

(2) Initial Electrical / Optical Characteristics <u>Table 7</u> (Table 7)						Ta=25 <b>°C</b> )
Item	Symbol	Condition	MIN	ТҮР	MAX	unit
Forward Voltage	VF	IF=20mA	-	(3.2)	3.5	V
Reverse Current	IR	VR=5V		-	50	μA

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#### (5-3) Interface signals

		Table 8			
Pin No	Symbol	Description	I/O		Remark
1	VSS	Ground level pin	-		-
2	VSS	Ground level pin	-		-
3	VEE	VEE level pin	-		For LCD driving
4	D15	Data Bus (MSB)	I/O		(Note 1)
5	D14	Data Bus	I/O		(Note 1)
6	D13	Data Bus	I/O		(Note 1)
7	D12	Data Bus	I/O		(Note 1)
8	D11	Data Bus	I/O		(Note 1)
9	D10	Data Bus	I/O		(Note 1)
10	D9	Data Bus	I/O		(Note 1)
11	D8	Data Bus	I/O		(Note 1)
12	VSS	Ground level pin	-		-
13	D7	Data Bus	I/O		
14	D6	Data Bus	I/O		
15	D5	Data Bus	I/O		
16	D4	Data Bus	I/O		
17	D3	Data Bus	I/O		
18	D2	Data Bus	I/O		
19	D1	Data Bus	I/O		
20	D0	Data Bus (LSB)	I/O		
21	VSS	Ground level pin	-		
22	VSS	Ground level pin	-		
23	/WR	Write control input pin	Ι		"L" active
24	RS	Register select pin	Ι		
25	/CS	Chip select input pin	Ι		"L" active
26	/RES	Reset signal input pin	Ι		"L" active
27	VDD	VDD level pin	-		For Logic driving
28	LCDINT	Interrupt request to the host bus	0		(Note 2)
29	/RD	Read control input pin	Ι		"L" active
30	IFM0	Selection signal pin for host interface	Ι	L	RS "H" : commands
		mode		H	RS "L" : commands
31	BUS0	Selection signal pin for the width of data bus	Ι	L H	8bit bus interface16bit bus interface
32	AN	LED back light for (Anode)	-		-
33	AN	LED back light for (Anode)	_		-
34	CA	LED back light for (Cathode)	-		-
35	CA	LED back light for (Cathode)	-	1	-

Used connection : 0.3mm pitch ZIF FPC connector.

Correspondable connector : FF02B35SS1 (JAE)

(Note 1) For unused Data Bus, connect to VSS.

(Note 2) If don't use "LCDINT" pin, leave it open.

Harrishow Harr	HA	<b>S</b> Þ	SPEC No. LCP-05032A	MODEL NO. LQ022B8UD05	PAGE	11
NWR       Image: Two the system of the transformation of the transfor		-				
RS NCS NCS NCS NCS NCS NCS NCS NC	wr –			Т <sub>WK2</sub>	▶	
IRD Fig.3 Host interface timing (Write) Fig.3 Host interface timing (Write) Fig.3 Host interface timing (Write) Table 9 Symbol Description Min. Max. Not Twee High period of NV/R 60 ns - Twee High period of NV/R 80 ns - Twee Prohibit time re-writing 140 ns - Twes Set up time of DB, RS and NCS to the NV/R rising. 50 ns - Twee Hold time of DB, RS and NCS to the NV/R rising. 0 ns - Twee Hold time of DB, RS and NCS to the NV/R rising. 0 ns - Twee Twee 300 ns - Twee Hold time of DB, RS and NCS to the NV/R rising. 0 ns - Twee Twee 300 ns -	ов –	₹	Valid	Valid		
IRD       Fig. 3 Host interface timing (Write)         Fig. 3 Host interface timing (Write)         Table 9         Symbol       Description       Min.       Max.       No         TwpL       Low period of NWR       60 ns       -       -         TwpH       High period of NWR       80 ns       -       -         Twc       Prohibit time re-writing       140 ns       -       -         Tws       Set up time of DB, RS and NCS to the NWR rising.       50 ns       -       -         Tws       Set up time of DB, RS and NCS to the NWR rising.       0 ns       -       -         Twkt       Hold time of DB, RS and NCS to the NWR rising.       0 ns       -       -         Twkt       Required time from the read cycle to write cycle       300 ns       -       -	RS		Valid	Valid	<u>,                                    </u>	
IRD       Fig. 3 Host interface timing (Write)         Fig. 3 Host interface timing (Write)         Table 9         Symbol       Description       Min.       Max.       No         TwpL       Low period of NWR       60 ns       -       -         TwpH       High period of NWR       80 ns       -       -         Twc       Prohibit time re-writing       140 ns       -       -         Tws       Set up time of DB, RS and NCS to the NWR rising.       50 ns       -       -         Tws       Set up time of DB, RS and NCS to the NWR rising.       0 ns       -       -         Twkt       Hold time of DB, RS and NCS to the NWR rising.       0 ns       -       -         Twkt       Required time from the read cycle to write cycle       300 ns       -       -	_	/≯	f\/`	<u> </u>		
SymbolDescriptionMin.Max.No.T_WPLLow period of NWR60 ns-T_WPHHigh period of NWR80 ns-T_WcProhibit time re-writing140 ns-T_WsSet up time of DB, RS and NCS to the NWR rising.50 ns-T_WHHold time of DB, RS and NCS to the NWR rising.0 ns-T_WK1Required time from the read cycle to write cycle300 ns-	-					
T_WPLLow period of NWR60 ns-T_WPHHIgh period of NWR80 ns-T_WCProhibit time re-writing140 ns-T_WSSet up time of DB, RS and NCS to the NWR rising.50 ns-T_WHHold time of DB, RS and NCS to the NWR rising.0 ns-T_WK1Required time from the read cycle to write cycle300 ns-	-	Fig.3		(Write)		
TWPH       High period of NWR       80 ns       -         Twc       Prohibit time re-writing       140 ns       -         Tws       Set up time of DB, RS and NCS to the NWR rising.       50 ns       -         TwH       Hold time of DB, RS and NCS to the NWR rising.       0 ns       -         TwK1       Required time from the read cycle to write cycle       300 ns       -	RD	-	Table 9	· · ·		
Twc       Prohibit time re-writing       140 ns       -         Tws       Set up time of DB, RS and NCS to the NWR rising.       50 ns       -         TwH       Hold time of DB, RS and NCS to the NWR rising.       0 ns       -         TwK1       Required time from the read cycle to write cycle       300 ns       -	RD Symbol	Des	Table 9	Min.		Note
T <sub>WS</sub> Set up time of DB, RS and NCS to the NWR rising.       50 ns       -         T <sub>WH</sub> Hold time of DB, RS and NCS to the NWR rising.       0 ns       -         T <sub>WK1</sub> Required time from the read cycle to write cycle       300 ns       -	RD Symbol T <sub>WPL</sub>	Des Low period of NWR	Table 9	<b>Min.</b> 60 ns	-	Note
T <sub>WH</sub> Hold time of DB, RS and NCS to the NWR rising.     0 ns     -       T <sub>WK1</sub> Required time from the read cycle to write cycle     300 ns     -	RD Symbol T <sub>WPL</sub> T <sub>WPH</sub>	Des Low period of NWR HIgh period of NWR	Table 9	Min. 60 ns 80 ns	-	Note
T <sub>WK1</sub> Required time from the read cycle to write cycle 300 ns -	RD Symbol T <sub>WPL</sub> T <sub>WPH</sub> T <sub>WC</sub>	Des Low period of NWR HIgh period of NWR Prohibit time re-writing	Table 9	Min. 60 ns 80 ns 140 ns	-	Note
	RD Symbol T <sub>WPL</sub> T <sub>WPH</sub> T <sub>WC</sub> T <sub>WS</sub>	Des Low period of NWR HIgh period of NWR Prohibit time re-writing Set up time of DB, RS and NCS	Table 9 cription	Min. 60 ns 80 ns 140 ns 50 ns	-	Note
	RD Symbol T <sub>WPL</sub> T <sub>WPH</sub> T <sub>WC</sub> T <sub>WS</sub> T <sub>WH</sub>	Des Low period of NWR HIgh period of NWR Prohibit time re-writing Set up time of DB, RS and NCS Hold time of DB, RS and NCS t	<u>Table 9</u> cription S to the NWR rising. to the NWR rising.	Min. 60 ns 80 ns 140 ns 50 ns 0 ns	-	Note
Twk2Required time from the write cycle to read cycleSoo isConditions: $V_{DDIOH} = 1.65 V$ to 3.3 V, $V_{DDCORE} = 1.8 \pm 0.15 V$ , Topr = - 30°C to +70°C, $C_L = 10 \text{ pF}$ Reference input voltage: $V_{IH} = 0.9 V_{DDIOH}, V_{IL} = 0.1 V_{DDIOH}$ Reference output voltage: $V_{OH} = 0.9 V_{DDIOH}, V_{OL} = 0.1 V_{DDIOH}$	RD Symbol T <sub>WPL</sub> T <sub>WPH</sub> T <sub>WC</sub> T <sub>WS</sub> T <sub>WH</sub> T <sub>WK1</sub>	Des Low period of NWR HIgh period of NWR Prohibit time re-writing Set up time of DB, RS and NCS Hold time of DB, RS and NCS to Required time from the read cy	Table 9 cription S to the NWR rising. to the NWR rising. rcle to write cycle	Min.           60 ns           80 ns           140 ns           50 ns           0 ns           300 ns	-	Note

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(2) Read			
RS T <sub>RSRS</sub>	x t t	Valid	
DB	Read data	Read data	
NWR			*
Fig.4	Host interface timing	(Read)	

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Symbol	Description	Min.	Max.
T <sub>RPL</sub>	Low period of NRD	100ns	-
T <sub>RPH</sub>			-
T <sub>RC</sub>	Prohibition time for re-reading	200ns	
T <sub>RSRS</sub>	Set up time of RS to NRD falling	50ns	-
T <sub>RSCS</sub>	Set up time of NCS to NRD falling	50ns	-
T <sub>RHRS</sub>	Hold time of RS from NRD falling	50ns	-
T <sub>RHCS</sub>	Hold time of NCS from NRD rising	50ns	-
T <sub>RDD</sub>	Time from NRD falling to confirmation of DB output	-	80ns
T <sub>RDH</sub>	Time from NRD rising to confirmation of DB output $1.65 \text{ V}$ to $3.3 \text{ V}$ V = $-5.18 \pm 0.15 \text{ V}$ Tapp = $-20\%$ to $\pm 70\%$ C	5ns	-

 $Conditions: \quad V_{\text{DDIOH}} = 1.65 \text{ V to } 3.3 \text{ V}, \\ V_{\text{DDCORE}} = 1.8 \pm 0.15 \text{ V}, \\ \text{Topr} = -30^{\circ}\text{C to } +70^{\circ}\text{C}, \\ \text{C}_{\text{L}} = 10 \text{ pF} \\ \text{Reference input voltage:} \qquad V_{\text{IH}} = 0.9 \text{ V}_{\text{DDIOH}}, \\ \text{V}_{\text{IL}} = 0.1 \text{ V}_{\text{DDIOH}} \\ \text{Reference output voltage:} \qquad V_{\text{OH}} = 0.9 \text{ V}_{\text{DDIOH}}, \\ \text{V}_{\text{OL}} = 0.1 \text{ V}_{\text{DDIOH}} \\ \end{array}$ 



Fig.5 Schematic of LCD module system



#### (5-6) Power ON/OFF sequence

#### (1) Power ON

Register	Command	Table 11 Remarks			
FD	FD	Software reset			
FD	FD				
		WAIT (Min 50ms)			
E0	01	Gate reset			
		WAIT (Min 5µs)			
E0	00	Gate reset release			
FE	FE	Host reset			
FE	FE				
EE	00	EEPROM I/F ready [Note]			
		WAIT (Min 10ms)			
EF	00	CPU bank active			
10	08	Host Interface setting register (1)			
12	AF	VRAM access area setting register (X direction/start and pointer)			
13	DB	VRAM access area setting register (Y direction/start and pointer)			
15	00	VRAM access area setting register (X direction/end)			
16	00	VRAM access area setting register (Y direction/end)			
18	03	Address auto increment setting register			
88	00	Display displaying color setting register			
7E	04	Display displaying setting register			
		WAIT (Min 20ms)			
7E	05	Display displaying setting register			
7F	01	V sync parameter transfer flag			
		[Write VRAM]			
80	01	Display displaying control register (DIPS ON)			

[Note]

A setup peculiar value to a panel is written in EEPROM.

[Cautions] Please do not rewrite



#### (2) Power OFF

		<u>Table 12</u>		
Register	Command	Remarks		
EF	00	CPU bank active		
1B	04	Host reset enable		
FE	FE	Host reset		
FE	FE			
7E	04	Display setting		
E3	04	Dc setting		
E4	04	Dc setting		
E2	01	Dc off setting		
80	00	Display Off		
E0	01	Gate reset		
7F	01	TG parameter refresh		
		WAIT (MIN 5 $\mu$ s)		
E0	00	Gate reset release		
7F	01	TG parameter refresh		
		WAIT (MIN 5 $\mu$ s)		
01	01	Oscillator stop		
		[Power off]		

#### 6. Optical Characteristics

					Table 13	1	1		Ta =25°C
Mode	parameter		symbol	conditio	MIN	ТҮР	MAX	unit	Remark
				n					
Tra	Brightness		В	θ=0°	88	125	-	cd/m <sup>2</sup>	Note 1,2
nsm	Contrast		Co	θ=0°	40:1	60:1	-		Note 1,3
issiv	Transm Contrast Viewing Angle		θу-	Co > 5	20	30	-	deg	Note 1
e			θy+		20	30	-		
			θx-		20	30	-		
			$\theta x +$		20	30	-		
	Response	Rise	τrl	θ=0°	-	18	35	ms	Note 1,4
	Time	Decay	τdl		-	45	75	ms	
	White chromaticity		x	θ=0°	-	0.31	-		Note 1,3
			у		-	0.35	-		
Ref	Reflectance		Rf	θ=0°	-	11	-	%	Note 5
Reflective	White chromaticity		x	θ=0°	-	0.30	-		Note 5
ive			у		-	0.34	-		

Note 1) Definition of range of visual angle



Fig.6 Definition of viewing angle

SHARP	SPEC No. LCP-05032A	MODEL No. LQ022B8UD05	page 17
Note 2) Brightness is measured as shown in Fi at the center of display area on optimu	•	the brightness of all pixels "Whit	te"
	SR-3	Measurement equipment: TOPCON(SR-3) Measuring spot size 4.9 mm Measuring field 1.0°	n <b>φ</b> ,

LCD Model

Diffuser

Light source

Fig.7 Optical characteristics Test Method (Brightness)

Note 3) Contrast ratio is defined as follows:

Luminance(brightness) all pixcels "White"

Luminance(brightness) all pixcels "dark"

Note 4) Response time is defined as follows:



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Note 5) Reflectance is defined as follows:			
Normal			
Diffusion light LCD panel of	(Inclus sensiti Diffusion light	Addetector ded a viewing vity modulator) Measurement equipment : LCD5200(Ohtsuka)	

Fig.9 Optical Characteristics Test Method

SHARP		SPEC No. LCP-05032A	MODEL NO. LQ022B8UI	D05 PAGE 19
7. Lot Number identificat Lot numbering and locat 1 2 3 05 L 00000 USP 5280371	ion are specified as	s follows. 6		
<ul> <li>①product year (low 05:2005, 06:200</li> <li>②product month A:JANUARY,B:J</li> <li>③Serial number</li> </ul>	06	RCHL:E	DECEMBER	
$000001 \sim 999$ (4) Record of Revision	n			
A:The first edition (5) product maker SC:SHARP (6) Used Patent N	on, B:Second editio	)n		
<ul> <li>8. Packing specifications (8-1) Details of packing</li> <li>1) Packing materials</li> </ul>		2) Packing	style :Fig.11	
(8-2) Reliability	.14010.15	2) I acking	Style .11g.11	
1) Vibration test		Table.1	4	
Item			est	
Frequency				
Direction				
Period	Up-Dow	Left-Right	Front-Back	Total
	60min	15min	15min	90min
The frequency should	l start at 5 Hz and	vary continuously.		
Total amplitude 20	0mm 0.2mm	20mm 0.2m	nm	
	Hz 50Hz $\bigcirc$ $\bigcirc$ $\leftarrow$ 3 minutes	5Hz 50H $\bigcirc$ $\rightarrow$	z (For 9.8m/s <sup>2</sup> )	
2) Drop test	Jinnutes	I		
	_			

Drop height: 750mm

Number of drop: 10timers (Ddrop sequence: 1 corner, 3 edges, 6 faces)



#### (8-3)Packing quantities

250 modules (max) per master carton

(8-4)Packing weight

About 7.7kg

#### (8-5)Paking outline dimensions

382mm × 578mm × 255mm

(Packi	acking materials)		Table.15
		Parts name	Materials
	1	Master carton	Corrugate card board
	2	Under pad	Corrugate card board
	3	Inside sleeve	Corrugate card board
	4	Outside sleeve	Corrugate card board
	5	Tray for packing	Polystyrene with anti-static treatment +anti-static polystyrene
	6	OPP tape	Polypropylene
	7	Protective bag	Polyethylene with anti-static treatment +anti-static polyethylene



Fig.10



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PAGE

#### 9. LCD module outline



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Fig. 12

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